National Semiconductor

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1 disp.

LM1889 TV Video Modulator

General Description

The LM1889 is designed to interface audio, color difference, and luminance signals to the antenna terminals of a TV receiver. It consists of a sound subcarrier oscillator, chroma subcarrier oscillator, quadrature chroma modulators, and RF oscillators and modulators for two low-VHF channels.

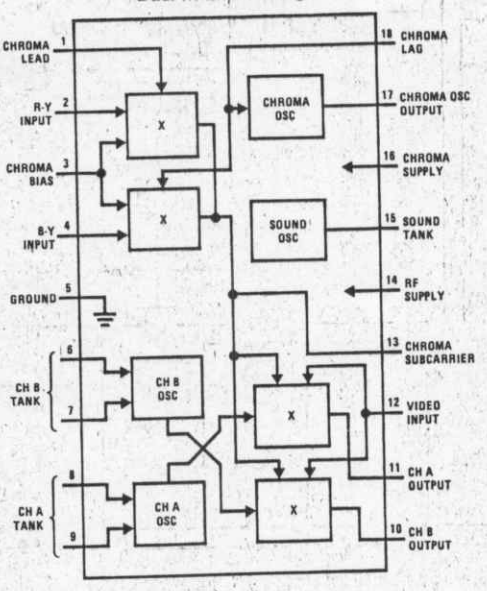
The LM1889 allows video information from VTR's, games, test equipment, or similar sources to be displayed on black and white or color TV receivers. When used with the MM57100 and MM53104, a complete TV game is formed.

Features

- dc channel switching
- 12V to 18V supply operation
- Excellent oscillator stability
- Low intermodulation products
- 5 Vp-p chroma reference signal
- May be used to encode composite video

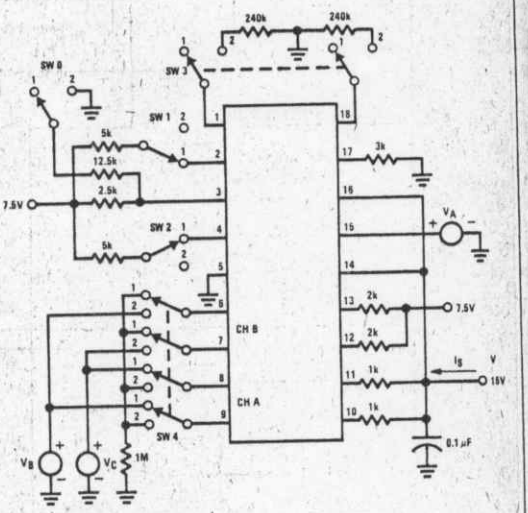
Block Diagram

Dual-In-Line Package



Order Number LM1889N
See NS Package N18A

DC Test Circuit



bsolute Maximum Ratings

pply Voltage V14, V16 max	19 V_{dc}
wer Dissipation Package (Note 1)	1390 mW
erating Temperature Range	0°C to +70°C
rage Temperature Range	−55°C to +150°C
roma Osc Current I_{17} max	10 mA_{dc}
(V16–V15) max	±5 V_{dc}
(V14–V10) max	7V
(V14–V11) max	7V
d Temperature (Soldering, 10 seconds)	300°C

C Electrical Characteristics (dc Test Circuit, All SW Normally Pos. 1, V_A = 15V, $V_B = V_C$ = 12V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
upply Current, I_S		20	35	45	mA
ound Oscillator, Current Change, ΔI_{15}	Change V_A From 12.5V to 17.5V	0.3	0.6	0.9	mA
hroma Oscillator Balance, V17		9.5	11.0	12.5	V
hroma Modulator Balance, V13		7.0	7.4	7.8	V
-Y Modulator Output Level, ΔV13	SW 3, Pos. 2, Change SW 1 From Pos. 1 to Pos. 2	0.6	0.9	1.2	V
-Y Modulator Output Level, ΔV13	SW 3, Pos. 2, Change SW 2 From Pos. 1 to Pos. 2	0.6	0.9	1.2	V
hroma Modulator Conversion Ratio, ΔV13/ΔV3	SW 3, Pos. 2, Change SW 0 From Pos. 1 to Pos. 2. Divide ΔV13 by ΔV3	0.45	0.70	0.95	V/V
h. A Oscillator "OFF" Voltage, V8, V9	SW 4, Pos. 2	0.5	1.5	3.0	V
h. A Oscillator Current Level, I_9	V_B = 12V, V_C = 13V	2.5	3.5	5	mA
h. B Oscillator "OFF" Voltage, V6, V7		0.5	1.5	3.0	V
h. B Oscillator Current Level, I_6	SW 4, Pos. 2, V_B = 12V, V_C = 13V	2.5	3.5	5	mA
h. A Modulator Conversion Ratio, ΔV11/(V13–V12)	SW 1, SW 2, SW 3, Pos. 2, V_B = 12V, Change V_C From 13V to 11V For ΔV11 Divide By V13–V12	0.35	0.55	0.75	V/V
h. B Modulator Conversion Ratio, ΔV10/(V13–V12)	All SW, Pos. 2, V_B = 12V, Change V_C From 13V to 11V Divide as Above	0.35	0.55	0.75	V/V

C Electrical Characteristics (ac Test Circuit, V = 15V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
hroma Oscillator Output Level, V17	$C_{LOAD} \leq 20$ pF	4	5		Vp-p
ound Carrier Oscillator Level, V15	Loaded by RC Coupling Network	2	3	4	Vp-p
h. 3 RF Oscillator Level, V8, V9	Ch. Sw. Pos. 3, f = 61.25 MHz, Use FET Probe	200	350		mVp-p
h. 4 RF Oscillator Level, V6, V7	Ch. Sw. Pos. 4, f = 67.25 MHz, Use FET Probe	200	350		mVp-p

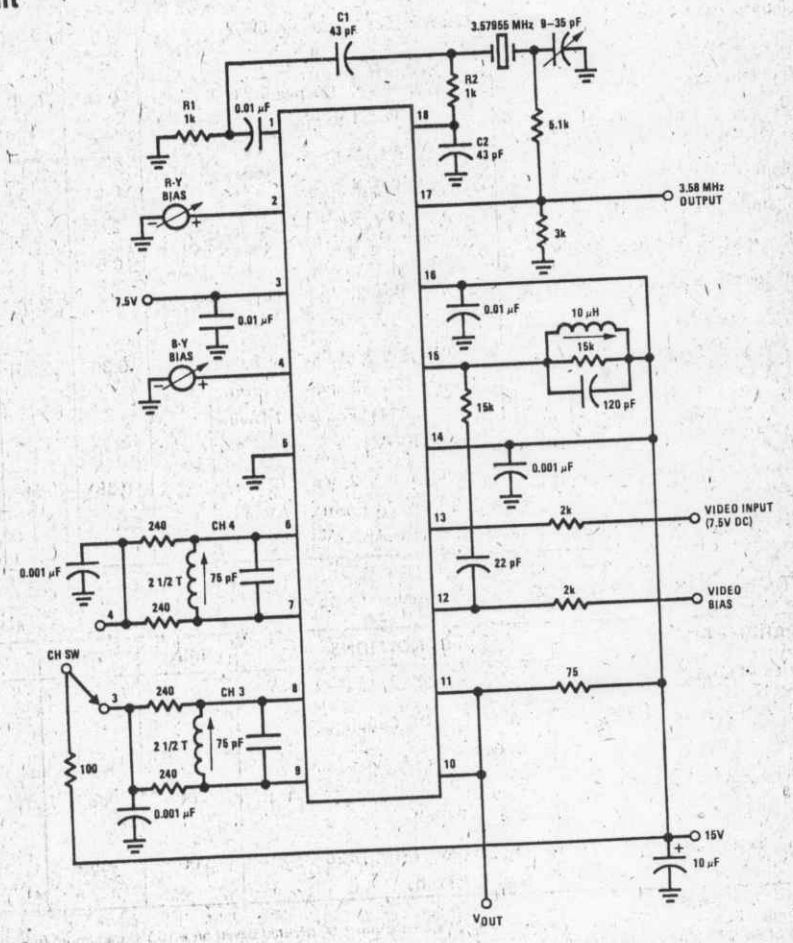
te 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a ermal resistance of 90°C/W junction to ambient.

Design Characteristics (ac Test Circuit, V = 15V)

PARAMETER	TYP	UNITS
Oscillator Supply Dependence		
Chroma, f_o = 3.579545 MHz	3	Hz/V
Sound Carrier, RF	See Curves	
Oscillator Temperature Dependence (IC Only)		
Chroma	0.05	ppm/°C
Sound Carrier	−15	ppm/°C
RF	−50	ppm/°C
Chroma Oscillator Output, Pin 17		
t_{RISE}, 10–90%	20	ns
t_{FALL}, 90–10%	30	ns
Duty Cycle (+) Half Cycle	51	%
(−) Half Cycle	49	%
RF Oscillator Maximum Operating Frequency (Temperature Stability Degraded)	100	MHz
Chroma Modulator (f = 3.58 MHz)		
B-Y Conversion Gain V13/(V4−V3)	0.6	Vp-p/V
R-Y Conversion Gain V13/(V2−V3)	0.6	Vp-p/V
Gain Balance	±0.5	dB
Bandwidth	See Curve	

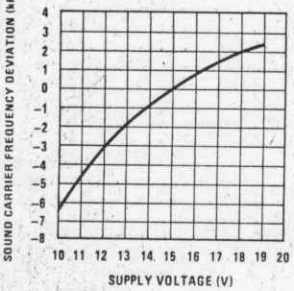
PARAMETER	TYP	UNITS
RF Modulator		
Conversion Gain, f = 61.25 MHz, $V_{OUT}/(V13-V12)$	10	mVrms/V
3.58 MHz Differential Gain	5	%
Differential Phase	3	degrees
2.5 Vp-p Video, 87.5% mod.		
Output Harmonics Below Carrier		
2nd, 3rd	−12	dB
4th and above	−20	dB
Input Impedances		
Chroma Modulator, Pins 2, 4	500k//2 pF	
RF Modulator, Pin 12	1M//2 pF	
Pin 13	250k//3.5 pF	

AC Test Circuit

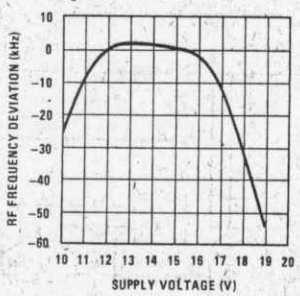


Typical Performance Characteristics

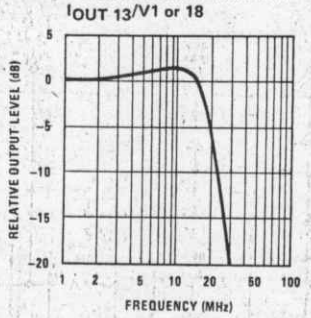
Sound Carrier Oscillator
Supply Dependence
(f_O = 4.5 MHz)



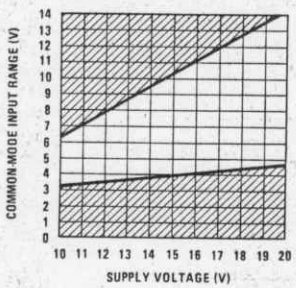
RF Oscillator Frequency
Supply Dependence
f_O = 67.25 MHz



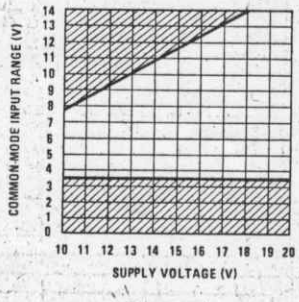
Chroma Modulator
Transconductance Bandwidth
$I_{OUT\ 13}/V1$ or 18



Chroma Modulator
Common-Mode Input Range
Pins 2, 3, 4



RF Modulator
Common-Mode Input Range
Pins 12, 13 (Applications Circuit)



Circuit Description (Refer to Circuit Diagram)

The sound carrier oscillator is formed by differential amplifier Q3, Q4 operated with positive feedback from the pin 15 tank to the base of Q4.

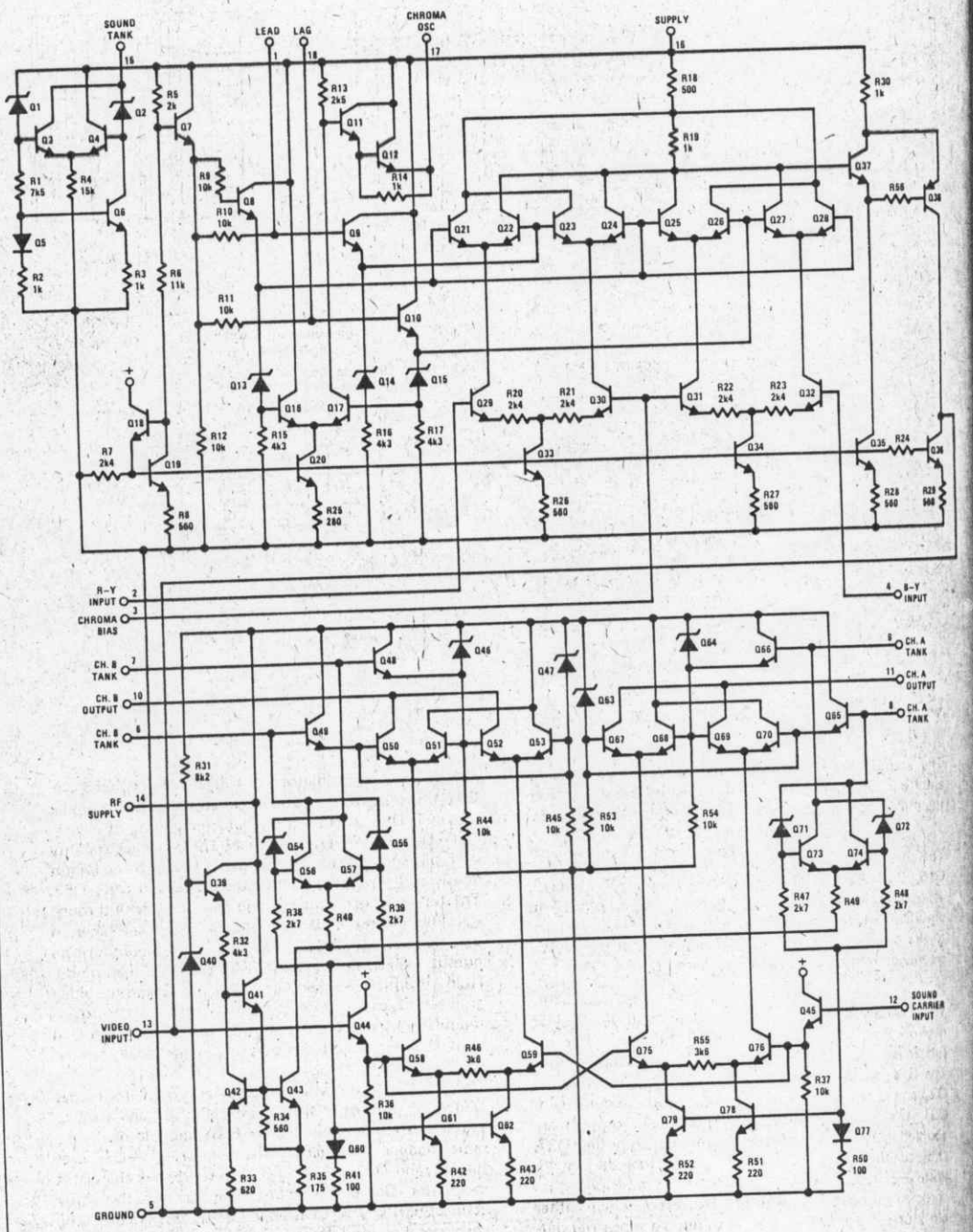
The chroma oscillator consists of the inverting amplifier Q16, Q17 and Darlington emitter follower Q11, Q12. An external RC and crystal network from pin 17 to pin 18 provides an additional 180 degrees phase lag back to the base of Q17 to produce oscillation at the crystal resonance frequency. (See ac test circuit).

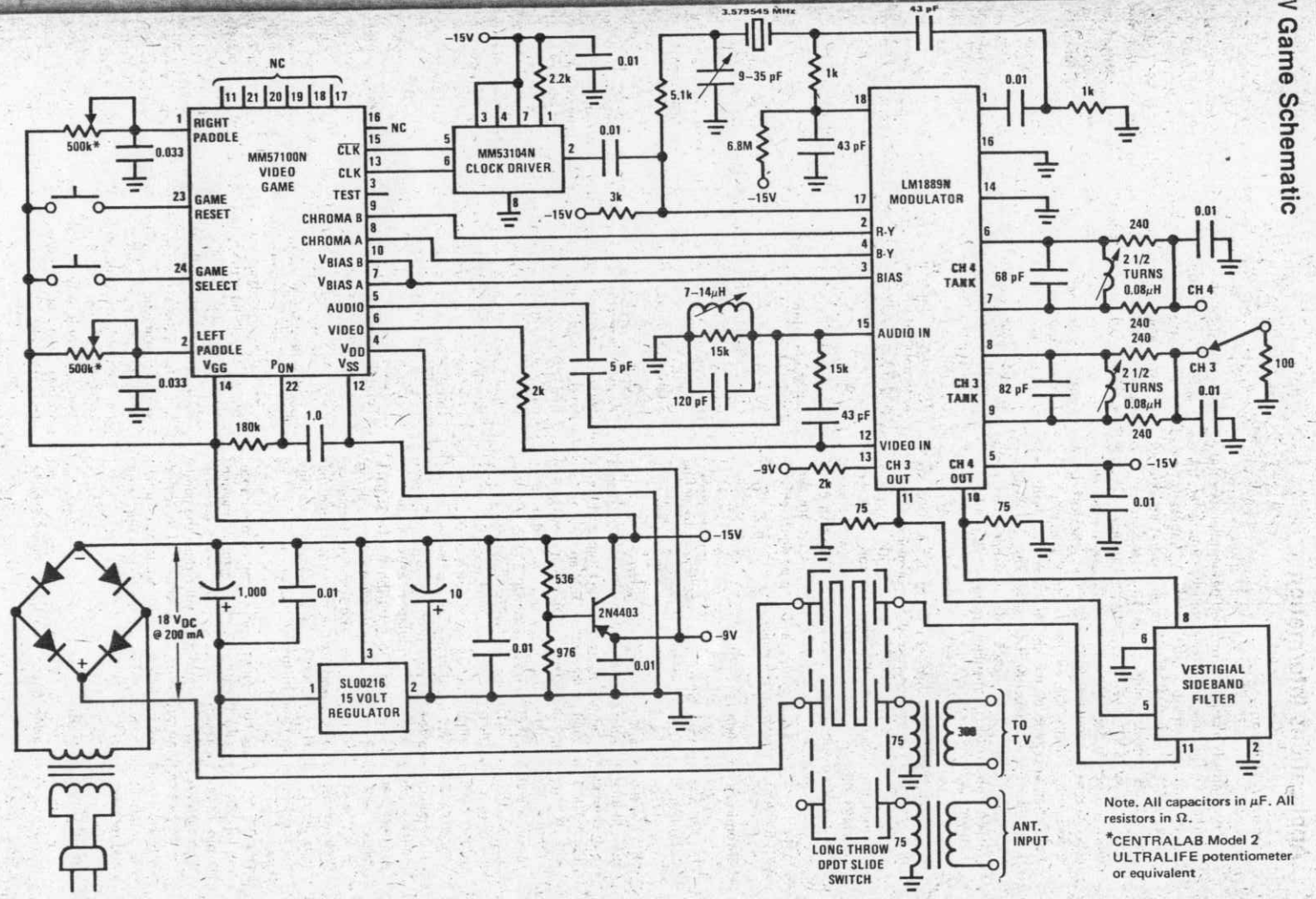
The feedback signal from the crystal is split in a lead-lag network to pins 1 and 18, respectively, to generate the subcarrier reference signals for the chroma modulators. The R-Y modulator consists of multiplier devices Q29, Q30 and Q21–Q24, while the B-Y modulator consists of Q31, Q32 and Q25–Q28. The multiplier outputs are coupled through a balanced summing amplifier Q37, Q38 to the input of the RF modulators at pin 13. With 0 offset at the lower pairs of the multipliers, no chroma output is produced. However, when either pin 2 or pin 4 is offset relative to pin 3 a subcarrier output current of the appropriate phase is produced at pin 13.

The channel B oscillator consists of devices Q56 and Q57 cross-coupled through level-shift zener diodes Q54 and Q55. A current regulator consisting of devices Q39–Q43 is used to achieve good RF frequency stability over supply and temperature. The channel B modulator consists of multiplier devices Q58, Q59 and Q50–Q53. The top quad is coupled to the channel B tank through isolating devices Q48 and Q49. A dc offset between pins 12 and 13 offsets the lower pair to produce an output RF carrier at pin 10. That carrier is then modulated by both the chroma signal at pin 13 and the video and sound carrier signals at pin 12. The channel A modulator shares pin 12 and 13 buffers Q45 and Q44 with channel B and operates in an identical manner.

The current flowing through channel B oscillator diodes Q54, Q55 is turned around in Q60, Q61 and Q62 to source current for the channel B RF modulator. In the same manner, the channel A oscillator Q71–Q74 uses turn around Q77, Q78 and Q79 to source the channel A modulator. One oscillator at a time may be activated by connecting its tank to supply (see ac test circuit). The corresponding modulator is then activated by its current turn-around, and the other oscillator/modulator combination remains "OFF".

Circuit Diagram




MM57100N VIDEO GAME
RIGHT PADDLE
GAME RESET
GAME SELECT
LEFT PADDLE
CLK
TEST
CHROMA B
CHROMA A
VBIAS B
VBIAS A
AUDIO
VIDEO
VDD
VSS
VGG
PON
NC
MM53104N CLOCK DRIVER
LM1889N MODULATOR
R-Y
B-Y
BIAS
AUDIO IN
VIDEO IN
CH 3 OUT
CH 4 OUT
CH 3 TANK
CH 4 TANK
3.579545 MHz
500k*
0.033
2.2k
0.01
5.1k
9–35 pF
1k
43 pF
6.8M
3k
7–14μH
15k
120 pF
5 pF
2k
180k
1.0
240
2 1/2 TURNS 0.08μH
68 pF
82 pF
100
75
18 VDC @ 200 mA
1,000
10
536
976
2N4403
SL00216 15 VOLT REGULATOR
VESTIGIAL SIDEBAND FILTER
TO TV
ANT. INPUT
LONG THROW DPDT SLIDE SWITCH
Note. All capacitors in μF. All resistors in Ω.
*CENTRALAB Model 2 ULTRALIFE potentiometer or equivalent

Applications Information

Subcarrier Oscillator

The oscillator is a crystal-controlled design to ensure the accuracy and stability required of the subcarrier frequency for use with television receivers. Lag-lead networks (R2C2 and C1R1) define a quadrature phase relationship between pins 1 and 18 at the subcarrier frequency of 3.579545 MHz. Other frequencies can be used and where high stability is not a requirement, the crystal can be replaced with a parallel resonant L-C tank circuit—to provide a 2 MHz clock, for example. Note that since one of the chrominance modulators is internally connected to the feedback path of the oscillator, operation of the oscillator at other than the correct subcarrier frequency precludes chrominance modulation.

When an external subcarrier source is available or preferred, this can be used instead. For proper modulator operation, a subcarrier amplitude of 500 mVp-p is required at pins 1 and 18. If the quadrature phase shift networks shown in the application circuit are retained, about 1 Vp-p subcarrier injected at the junction of C1 and R2 is sufficient. The crystal, C4 and R3 are eliminated and pin 17 provides a 5 Vp-p signal shifted +125° from the external reference.

Chrominance Modulation

The simplest method of chroma encoding is to define the quadrature phases provided at pins 1 and 18 as the color difference axes R-Y and B-Y. A signal at pin 2 (R-Y) will give a chrominance subcarrier output from the modulator with a relative phase of 90° compared to the subcarrier output produced by a signal at pin 4 (B-Y). The zero signal dc level of the R-Y and B-Y inputs will determine the bias level required at pin 3. For example, a pin 2 signal that is 1V positive with respect to pin 3 will give 0.6 Vp-p subcarrier at a relative phase of 90°. If pin 2 is 1V negative with respect to pin 3, the output is again 0.6 Vp-p, but with a relative phase of 270°. When a simultaneous signal exists at pin 4, the subcarrier output level and phase will be the vector sum of the quadrature components produced by pin 2 and 4 inputs. Clearly, with the modulation axes defined as above, a negative pulse on pin 4 during the burst gate period will produce the chrominance synchronizing "burst" with a phase of 180°. Both color difference signals must be dc coupled to the modulators and the zero signal dc level of both must be the same and within the common-mode range of the modulators.

The 0.6 Vp-p/V_{dc} conversion gain of the chrominance modulators is obtained with a 2 kΩ resistor connected at pin 13. Larger resistor values can be used to increase the gain, but capacitance at pin 13 will reduce the bandwidth. Notice that equi-bandwidth encoding of the color difference signals is implied as both modulator outputs are internally connected and summed into the same load resistor.

Sound Oscillator

Frequency modulation is achieved by using a 4.5 MHz tank circuit and deviating the center frequency via a capacitor or a varactor diode. Switching a 5 pF capacitor to ground at an audio frequency rate will cause a 50 kHz deviation from 4.5 MHz. A 1N5447 diode biassed −4V from pin 16 will give ±20 kHz deviation with a 1 Vp-p audio signal. The coupling network to the video modulator input and the varactor diode bias must be included when the tank circuit is tuned to center frequency.

A good level for the RF sound carrier is between 2% and 20% of the picture carrier level. For example, if the peak video signal offset of pin 12 with respect to pin 13 is 3V, this corresponds to a 30 mVrms picture RF carrier. The source impedance at pin 12 is defined by the external 2 kΩ resistor and so a series network of 15 kΩ and 24 pF will give a sound carrier level at −32 dB to the picture carrier.

RF Modulation

Two RF channels are available, with carrier frequencies up to 100 MHz being determined by L-C tank circuits at pins 6, 7, 8 and 9. The signal inputs (pins 12, 13) to both modulators are common, but removing the power supply from an RF oscillator tank circuit will also disable that modulator.

As with the chrominance modulators, it is the offset between the two signal input pins that determines the level of RF carrier output. Since one signal input (pin 13) is also internally connected to the chrominance modulators, the 2 kΩ load resistor at this point should be connected to a bias source within the common-mode input range of the video modulators. However, this bias source is independent of the chrominance modulator bias and where chrominance modulation is not used, the 2 kΩ resistor is eliminated and the bias source connected directly to pin 13.

To preserve the dc content of the video signal, amplitude modulation of the RF carrier is done in one direction only, with increasing video (toward peak white) decreasing the carrier level. This means the active composite video signal at pin 12 must be offset with respect to pin 13 and the sync pulse should produce the largest offset (i.e., the offset voltage of pin 12 with respect to pin 13 should have the same polarity as the sync pulses).

The largest video signal (peak white) should not be able to suppress the carrier completely, particularly if sound transmission is needed. For example, a signal with 1V sync amplitude and 2.5V peak white (3.5 Vp-p – negative polarity sync) and a black level at 5 V_{dc} will require a dc bias of 8V on pin 13 for correct modulation. A simple way of obtaining the required offset is to bias pin 13 at 4 x (sync amplitude) from the sync tip level at pin 12.

Applications Information (Continued)

Split Power Supplies

The LM1889 is designed to operate over a wide range of supply voltages so that much of the time it can utilize the signal source power supplies. An example of this is shown in *Figure 2* where the composite video signal from a character generator is modulated onto an RF carrier for display on a conventional home TV receiver. The LM1889 is biased between the −12V and +5V supplies and pin 13 is put at ground. A 9.1 kΩ resistor from pin 12 to −12V, dc offsets the video input signal (which has sync tips at ground) to establish the proper modulation depth − R1/R2 = V_{IN}/12 x 0.875. This design is for monochrome transmission and features an extremely low external parts count.

DC Clamped Inputs

Utilizing a DC clamp will make matching the LM1889 to available signal generator outputs a simple process. *Figure 3* shows the LM1889 configured to accept the composite video patterns available from a Tektronix Type 144 generator that has black level at ground and negative polarity syncs. In this application, the chroma oscillator amplifier is used to provide a gain of two. The 100k pot adjusts the overall DC level of the amplified signal which determines the modulation depth of the RF output. Clamping the input requires a minimum of DC correction to obtain the correct DC output level. This allows the adjustment to be a high impedance that will have minimum effect on the amplifier closed loop gain.

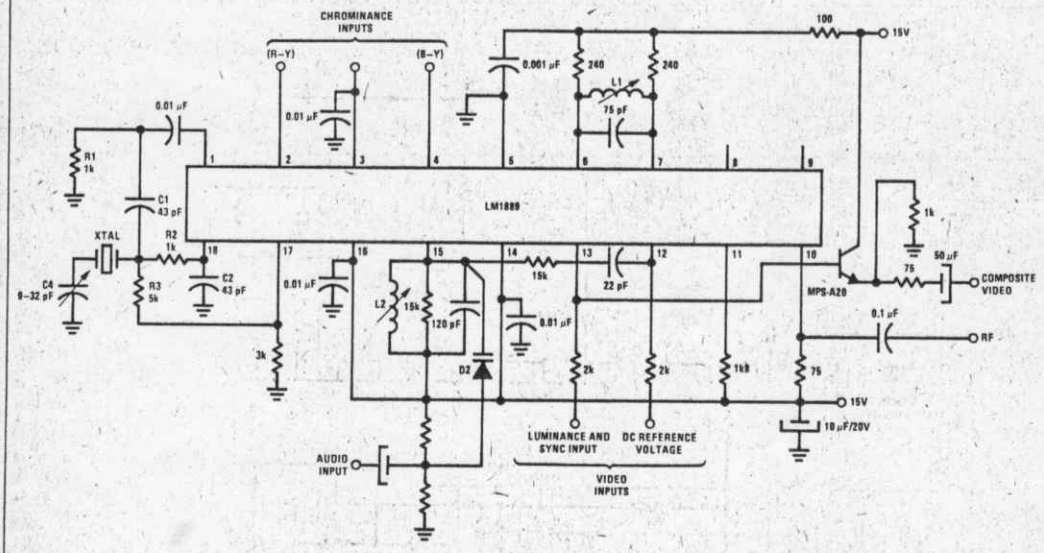


FIGURE 1. Luminance and Chrominance Encoding Composite Video or RF Output

Applications Information (Continued)

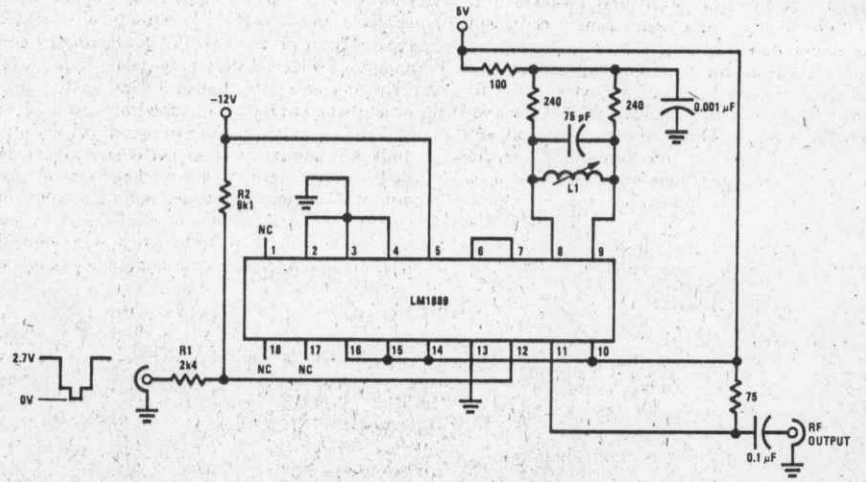


FIGURE 2. Low-Cost Monochrome Modulator for Character Generator Display

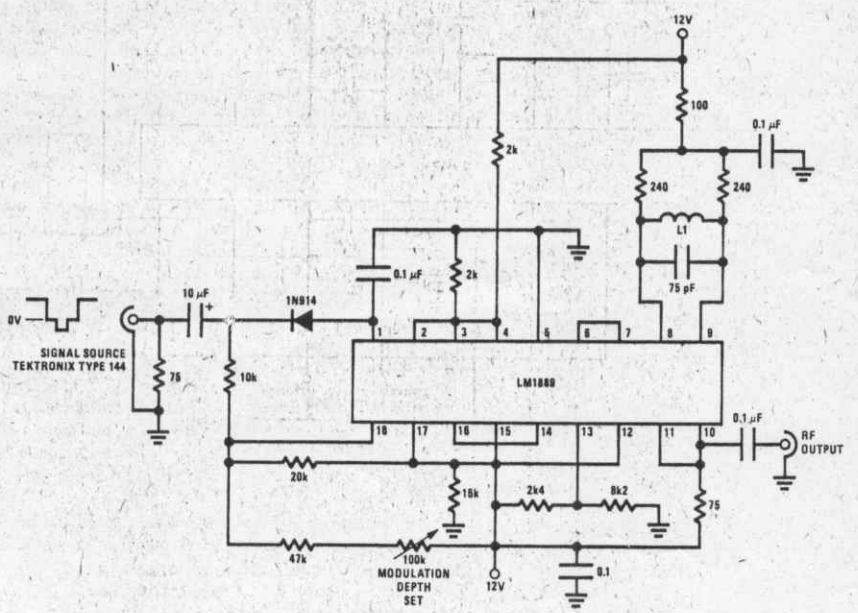
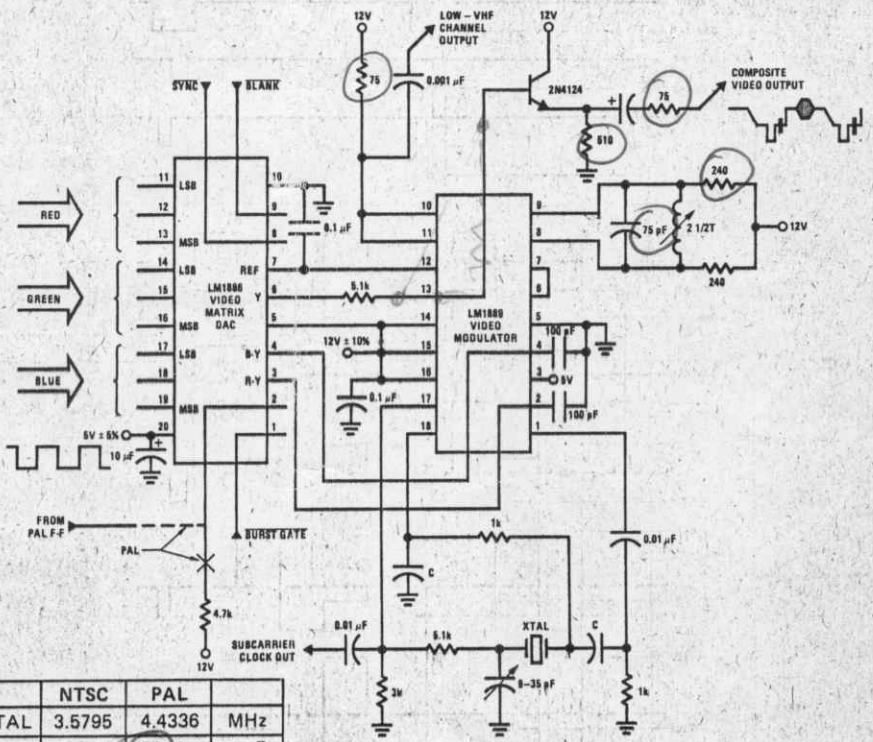


FIGURE 3. DC Clamped Modulator for NTSC Pattern Generators

Typical Application



	NTSC	PAL	
XTAL	3.5795	4.4336	MHz
C	43	36	pF

FIGURE 3

Circuit Description (Refer to *Figure 4*)

The 3-bit red, green, and blue inputs go to identical 3-bit current-mode digital-to-analog converters (DACs). Each DAC consists of three binary-weighted current sources controlled by diff-amp current switches. The DAC output currents are arbitrarily given a weighting factor of 0.59, which is the green coefficient in the luminance equation. Portions of the red and blue currents are split off, so that the remaining currents combined with the green current form the luminance current $I_Y = 0.3\ I_R + 0.59\ I_G + 0.11\ I_B$. I_Y develops the luminance voltage V_Y across R_O in a summing amplifier referenced to the +5V supply. A current switch operated by pin 8 adds (−) sync pulses to the Y output at pin 6.

The portions of red and blue currents previously split off flow through resistors $R_O/0.29$ and $R_O/0.48$, which are weighted to form the red and blue voltages respectively. Since the opposite ends of the 2 resistors are connected to V_Y, the red and blue voltages across the resistors subtract from V_Y to develop the color difference voltages V_{Y-R} and V_{Y-B}. V_{Y-B} is coupled through a X.56 gain, 5V-referenced inverting amplifier to the B-Y output at pin 4. V_{Y-R} feeds parallel inverting and non-inverting unity gain amplifiers which allow either polarity to be coupled to the R-Y output pin 3. Switching between the 2 amplifiers is controlled by a current switch activated by the H/2 pin 2. A (−) burst gate pulse on pin 1 controls current switches which add the burst pulse components to the B-Y and R-Y outputs.

The requirements for PAL and NTSC encoding differ in the areas of burst gate operation and R-Y polarity, both of which are controlled via pin 2 as follows:

PAL, pin 2 fed by a half-line frequency TTL square wave—in this mode a PNP switch between pin 2 and +5V is held off continuously, which results in equal burst pulse components on the B-Y and R-Y outputs. In addition, the H/2 square wave causes the R-Y output polarity to reverse every line. (When fed to the LM1889 chroma modulator this causes the phase of the R-Y subcarrier to change 180° as required in PAL.)

NTSC, pin 2 tied through an external resistor to +12V—this turns on the PNP switch continuously, which eliminates the burst pulse on the R-Y output and increases the amplitude of the B-Y pulse. Since pin 2 is being held high, the R-Y output is locked in the positive polarity.

Blanking is activated by a low on pin 9, which de-biases the left side of the DAC diff-amps, so that $I_R = I_G = I_B = 0$ independent of the input states. When blanked, the Y, B-Y and R-Y outputs all go to +5V. An additional amplifier produces a 0 carrier reference voltage at pin 7 which is 25% above the peak white voltage on the Y output, relative to +5V.

National Semiconductor

LM1886 TV Video Matrix D to A

General Description

The LM1886 is a TV video matrix D to A converter which encodes luminance and color difference signals from 3-bit red, green and blue inputs. The luminance output is encoded from the NTSC equation Y = 0.3R + 0.59G + 0.11B and the R-Y and B-Y outputs are weighted to prevent over-modulation. A built-in R-Y and burst gate polarity switch allow European PAL compatible signals to be encoded. All output levels including an RF O Carrier Bias Voltage have been referenced to 5V for direct connection to the LM1889 TV video modulator. When used in combination with the LM1889 and a suitable sync generator, 3-bit R, G and B information may be encoded to both composite video and RF channel carrier.

Features

- Complete digital to RF encoding with LM1889
- 1-pin PAL/NTSC mode select
- True NTSC matrix
- 8 levels of grey scale
- Allows wide range of colorimetry
- Low power TTL inputs
- Wideband luminance output
- Weighted R-Y, B-Y outputs

Connection Diagram

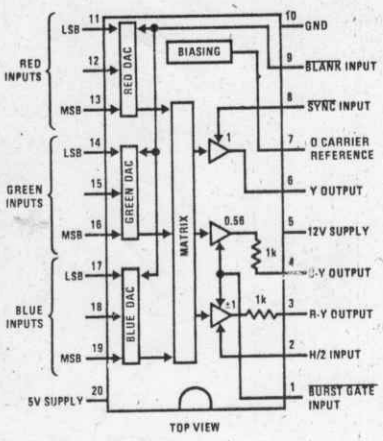


FIGURE 1

Order Number LM1886N
See NS Package N20A

Test Circuits

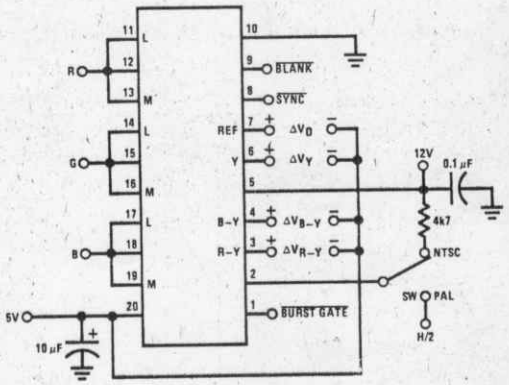


FIGURE 2a. 6-Color Input Connection

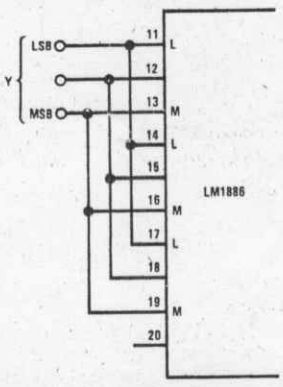


FIGURE 2b. 8-Level Grey Scale Input Connection

Absolute Maximum Ratings

Supply Voltage	
Pin 5	15V
Pin 20	6V
Input Voltage (Pins 1, 8, 9, 11–19)	−0.5V, +12V
Pin 2 Voltage Relative to Pin 20	0.8V
Output Current	5 mA
Power Dissipation, T_A = 25°C (Note 1)	1.67 W
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	0°C to 70°C
Lead Temperature (Soldering, 10 seconds)	300°C

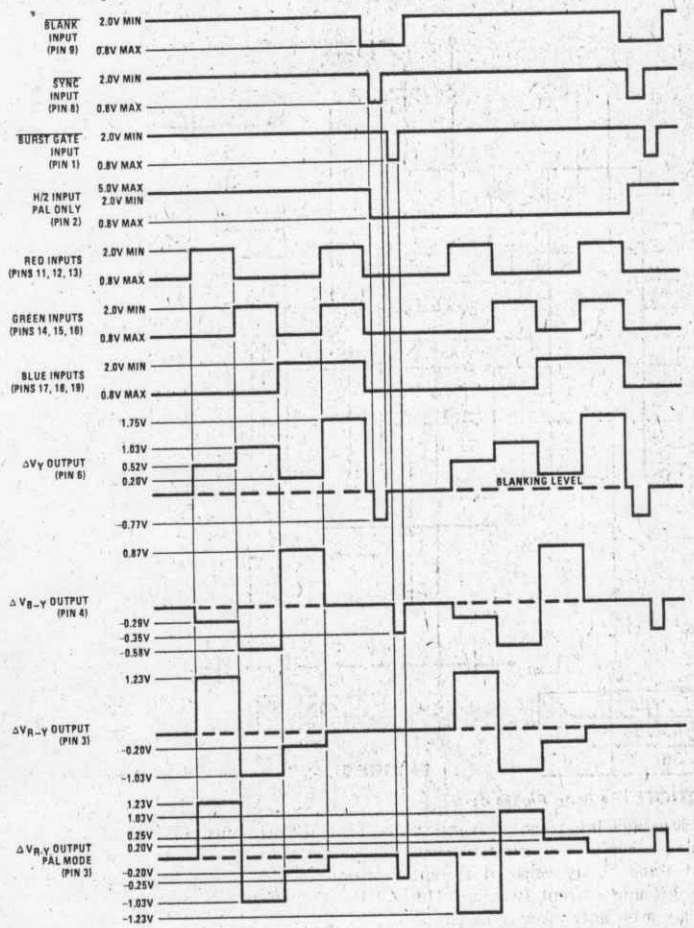
Electrical Characteristics T_A = 25°C, (*Figure 2*, Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
5V Supply Current (Pin 20)	$\overline{\text{BLANK}}$ = 0.8V	7	11	16	mA
12V Supply Current (Pin 5)	$\overline{\text{BLANK}}$ = 0.8V	9	13	17	mA
Logic "1" Input Current (Pins 1, 2, 8, 9, 11–19)	Input Voltage = 5.0V		0	10	μA
Logic "0" Input Current (Pins 1, 2, 8, 9, 11–19)	Input Voltage = 0.3V		−0.01	−0.18	mA
Output Offsets	R, G, B = 0.8V				
ΔV_Y			0	±50	mV
$\Delta V_{R\text{-}Y}$			0	±50	mV
$\Delta V_{B\text{-}Y}$			0	±50	mV
R-Y Full Scale, $(\Delta V_{R\text{-}Y})_{FS}$	R = 2V; G, B = 0.8V	1.0	1.23	1.4	V
B-Y Full Scale, $(\Delta V_{B\text{-}Y})_{FS}$	B = 2V; R, G = 0.8V	0.7	0.87	1.0	V
Green Full Scale	G = 2V: R, B = 0.8V				
$\Delta V_{R\text{-}Y}$		−0.85	−1.03	−1.2	V
$\Delta V_{B\text{-}Y}$		−0.45	−0.58	−0.7	V
Y Full Scale	R, G, B = 2V				
$(\Delta V_Y)_{FS}$		1.6	1.75	1.9	V
$\Delta V_{R\text{-}Y}$			0	±100	mV
$\Delta V_{B\text{-}Y}$			0	±75	mV
O Carrier Reference, ΔV_O		2.0	2.2	2.5	V
Blanking Level, ΔV_Y	$\overline{\text{BLANK}}$ = 0.8V		0	±50	mV
Sync Level, ΔV_Y	$\overline{\text{BLANK}}$, $\overline{\text{SYNC}}$ = 0.8V	−0.67	−0.77	−0.87	V
NTSC Burst, $\Delta V_{B\text{-}Y}$	$\overline{\text{BLANK}}$, $\overline{\text{BURST GATE}}$ = 0.8V	−0.26	−0.35	−0.46	V
PAL Burst					
$\Delta V_{R\text{-}Y}$	SW in PAL Position;	−0.2	−0.25	−0.32	V
$\Delta V_{B\text{-}Y}$	$\overline{\text{BLANK}}$, $\overline{\text{BURST GATE}}$, H/2 = 0.8V	−0.2	−0.25	−0.32	V
PAL Inversion Ratio $(\Delta V_{R\text{-}Y})_{PAL}/(\Delta V_{R\text{-}Y})_{FS}$	R = 2V; G, B, H/2 = 0.8V SW to PAL Position	−0.9	−1.0	−1.1	
Y Linearity Error	*Figure 2b* Input Connection		±1	±6	%FS
Y Switching Times	15 kHz Square Wave Switching R, G, B in Parallel				
Rise Time, t_R			35		ns
Fall Time, t_F			30		ns
Settling Time ±1 LSB			50		ns

Note 1: Above T_A = 25°C, derate based on $T_{J(MAX)}$ = 150°C and θ_{JA} = 75°C/W.

Note 2: Unless otherwise noted, $\overline{\text{BLANK}}$, $\overline{\text{SYNC}}$, $\overline{\text{BURST GATE}}$ = 2V and SW is in NTSC position. All outputs are referenced to the +5V supply as shown in *Figure 2a*.

Typical Input and Output Waveforms



Application Notes (Refer to *Figure 3*)

$\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$, and $\overline{\text{BURST GATE}}$ may be obtained from a sync generator IC similar to MM5320 or MM5321. For PAL operation, the H/2 square wave may be obtained by a ÷2 from horizontal sync.

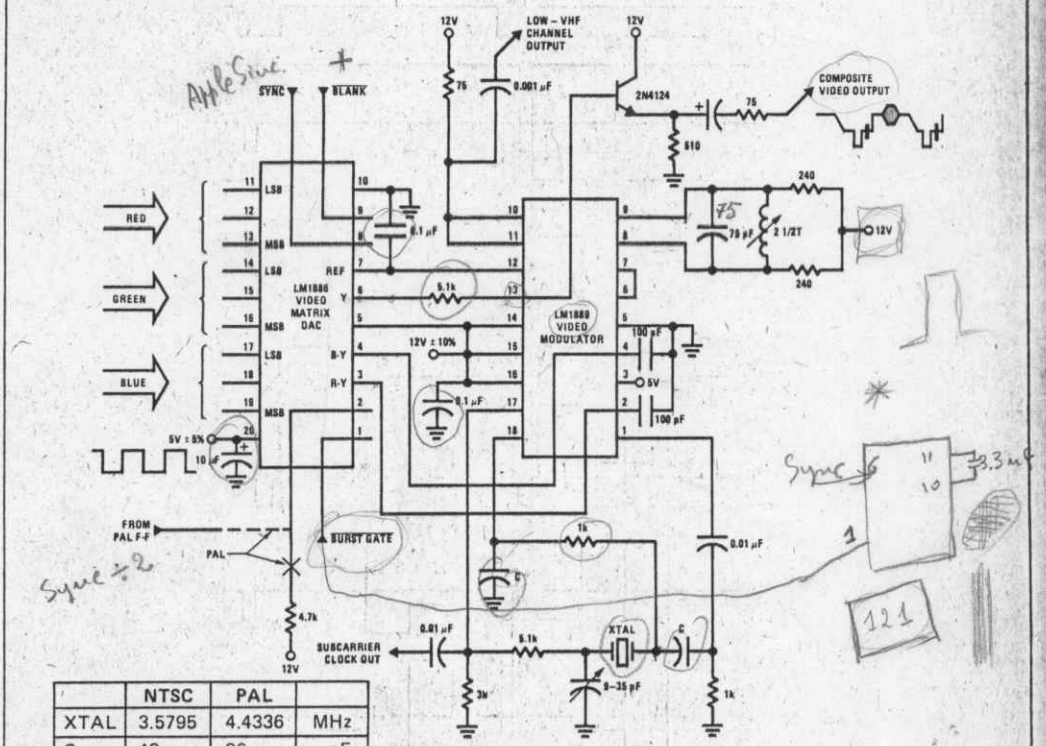
All inputs are low-power TTL compatible. Because of the very low typical input currents, the color inputs may be paralleled in various combinations. For simple color requirements, the *Figure 2a* input connection may be used to produce the 6 primary and complementary colors listed in Table I, along with black and white. To add complex colors such as those at the bottom of Table I, all 9 input bits may be required separately. When choosing input codes for other colors, always check the new color against both light and dark backgrounds.

All outputs are referenced to the +5V supply for direct connection to the LM1889. The resistor on the luminance output pin 6 is used to sum the chroma subcarrier from the LM1889 and must be wired as tightly as possible to preserve the video bandwidth. For the addition of sound or a second RF channel, refer to the LM1889 data sheet.

TABLE I. INPUT CODE EXAMPLES FOR COMMON COLORS

		INPUT CODE					
		RED		GREEN		BLUE	
	COLOR	M	L	M	L	M	L
	Black	0 0 0		0 0 0		0 0 0	
	Dark Grey	0 1 0		0 1 0		0 1 0	
	Light Grey	1 0 1		1 0 1		1 0 1	
	White	1 1 1		1 1 1		1 1 1	
Primary	Red	1 1 1		0 0 0		0 0 0	
Primary	Green	0 0 0		1 1 1		0 0 0	
Primary	Blue	0 0 0		0 0 0		1 1 1	
Complementary	Cyan	0 0 0		1 1 1		1 1 1	
Complementary	Magenta	1 1 1		0 0 0		1 1 1	
Complementary	Yellow	1 1 1		1 1 1		0 0 0	
	Brown	0 1 1		0 1 1		0 0 0	
	Orange	1 1 1		1 0 0		0 0 0	
	Flesh tone	1 1 1		1 1 0		1 0 1	
	Pink	1 1 1		1 1 0		1 1 0	
	Sky Blue	1 0 1		1 0 1		1 1 1	

Typical Application



	NTSC	PAL	
XTAL	3.5795	4.4336	MHz
C	43	36	pF

FIGURE 3

Circuit Description (Refer to *Figure 4*)

The 3-bit red, green, and blue inputs go to identical 3-bit current-mode digital-to-analog converters (DACs). Each DAC consists of three binary-weighted current sources controlled by diff-amp current switches. The DAC output currents are arbitrarily given a weighting factor of 0.59, which is the green coefficient in the luminance equation. Portions of the red and blue currents are split off, so that the remaining currents combined with the green current form the luminance current $I_Y = 0.3\ I_R + 0.59\ I_G + 0.11\ I_B$. I_Y develops the luminance voltage V_Y across R_O in a summing amplifier referenced to the +5V supply. A current switch operated by pin 8 adds (−) sync pulses to the Y output at pin 6.

The portions of red and blue currents previously split off flow through resistors $R_O/0.29$ and $R_O/0.48$, which are weighted to form the red and blue voltages respectively. Since the opposite ends of the 2 resistors are connected to V_Y, the red and blue voltages across the resistors subtract from V_Y to develop the color difference voltages V_{Y-R} and V_{Y-B}. V_{Y-B} is coupled through a X.56 gain, 5V-referenced inverting amplifier to the B-Y output at pin 4. V_{Y-R} feeds parallel inverting and non-inverting unity gain amplifiers which allow either polarity to be coupled to the R-Y output pin 3. Switching between the 2 amplifiers is controlled by a current switch activated by the H/2 pin 2. A (−) burst gate pulse on pin 1 controls current switches which add the burst pulse components to the B-Y and R-Y outputs.

The requirements for PAL and NTSC encoding differ in the areas of burst gate operation and R-Y polarity, both of which are controlled via pin 2 as follows:

PAL, pin 2 fed by a half-line frequency TTL square wave—in this mode a PNP switch between pin 2 and +5V is held off continuously, which results in equal burst pulse components on the B-Y and R-Y outputs. In addition, the H/2 square wave causes the R-Y output polarity to reverse every line. (When fed to the LM1889 chroma modulator this causes the phase of the R-Y subcarrier to change 180° as required in PAL.)

NTSC, pin 2 tied through an external resistor to +12V—this turns on the PNP switch continuously, which eliminates the burst pulse on the R-Y output and increases the amplitude of the B-Y pulse. Since pin 2 is being held high, the R-Y output is locked in the positive polarity.

Blanking is activated by a low on pin 9, which de-biases the left side of the DAC diff-amps, so that $I_R = I_G = I_B = 0$ independent of the input states. When blanked, the Y, B-Y and R-Y outputs all go to +5V. An additional amplifier produces a 0 carrier reference voltage at pin 7 which is 25% above the peak white voltage on the Y output, relative to +5V.

Equivalent Schematic

FIGURE 4. LM1886 Equivalent Schematic